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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,857	12/22/2000	Richard P. Modelski	P 270188 NOR-13180BA	8573

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EXAMINER	
TRUONG, LAN DAI T	

ART UNIT	PAPER NUMBER
2152	

DATE MAILED: 06/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/741,857	MODELSKI ET AL.	
	Examiner	Art Unit	
	Lan-Dai Thi Truong	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/14/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is response to communications: application, filed 12/22/2000; amendment filed 02/21/2006. Claims 1-18 are pending; claims 1-5, 11-17 are amended

2. The applicant's arguments filed on 02/21/2006 have fully considered but they are moot in view with new ground for rejection

Claim rejections-35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or descry bed as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5 and 17 are rejected under 35 U.S.C 103(a) as being un-patentable over Davis et al. (U.S. 5,357,617) in view of Esponda et al. ("The RISC Concept – A Survey of Implementations," September 1991)

Regarding to claim 1:

Davis discloses the invention substantially as claimed, including a method, which can be implemented in a computer hardware or software code for processing a plurality of instruction threads, comprising:

Retrieving a first instruction from a first thread of instructions; retrieving a second instruction from a second thread of instructions: (Davis discloses a multiple-threads processor processes simultaneously concurrent multiple independent threads via single pipeline processor; wherein the single pipeline processor process simultaneously multiple instructions belong to independent registered threads: column 2, lines 1-9, lines 42-67; column 4, lines 36-54)

The first instruction and the second instruction can be executed simultaneously in the processing pipeline: (Davis discloses a method for simultaneously execution one instruction of one thread while executing one instruction of other thread: column 2, lines 42-67)

Independence of the instructions threads eliminates pipeline processing delays: (Davis discloses the multi-thread processor eliminates the delays: column 2, lines 1-9; column 8, lines 15-20)

However, Davis does not explicitly discloses method for executing the first instruction in a first stage of a processing pipeline; and forwarding the first instruction to a next stage of the processing while forwarding the second instruction to the first stage of the processing pipeline

In analogous art, Esponda discloses "instruction I" which is equivalent to "first instruction" and "instruction I+1" which is equivalent to "second instruction;" Esponda discloses the instruction I fetched into instruction fetch stage; then the instruction I is forward to the next stage decode while the instruction I+1 being fetched into instruction fetch stage: ("The RISC

Concept-A Survey of Implementations," Margarita Espoda, page 4, lines 42-44; page 5, lines 1-5)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Esponda's ideas of parallel executing multiple independent thread instructions with Davis's system in order to eliminate delay time, see (column 2, lines -10)

Regarding to claim 5:

Davis discloses the invention substantially as claimed, including an apparatus, which can be implemented in a computer hardware or software code for processing a plurality of instruction threads, comprising:

A processing pipeline receives and processes the plurality of independent instruction threads: (Davis discloses a single pipeline process the plurality of independent instruction threads: title; column 4, lines 36-58; column 2, lines 1-12, 42-67)

Independence of the instructions threads eliminates pipeline processing delays: (Davis discloses the multi-thread processor eliminates the delays: column 2, lines 1-9; column 8, lines 15-20)

However, Davis does not explicitly discloses a processing pipeline including a plurality of stages; during a processing period, each of plurality of stage of processing pipeline is operating on a different one of the instruction threads from the plurality of instruction threads

In analogous art, Esponda discloses "instruction I" which is equivalent to "first instruction" and "instruction I+1" which is equivalent to "second instruction;" Esponda discloses the instruction I fetched into instruction fetch stage; then the instruction I is forward to the next

stage decode while the instruction I+1 being fetched into instruction fetch stage: ("The RISC Concept-A Survey of Implementations," Margarita Espoda, page 4, lines 42-44; page 5, lines 1-5)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Esponda's ideas of parallel executing multiple independent thread instructions with Davis's system in order to eliminate delay time, see (column 2, lines -10)

Regarding to claim 17:

In addition to rejection in claim 5, Davis-Esponda further discloses each instruction thread is a thread identifier identifying a subset registers allocated to corresponding independent instruction threads, the subset of registers selected from among a set of registers, and wherein the subsets associated with each one of the plurality of independent instruction threads are unique: (Davis discloses multiple independent instruction threads register to multiple-threads processor: abstract, lines 4-9; column 5, lines 32-67; column 6, lines 1-60)

Claim 4 is rejected under 35 U.S.C 103(a) as being un-patentable over Davis-Esponda in view of Abel et al. (U.S. 6,768,716)

Regarding to claim 4:

Davis-Esponda discloses the invention substantially as disclosed in claim 1, but does not explicitly teach processing data at a rate of at least 10 Gbs

However, Abel discloses parallel processors support speed rate about 10 Gbs or more: (column 6, lines 8-16)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Abel's ideas of using processors support speed rate about 10 Gbs or more with Davis-Esponda's system in order to improve communication speed

Claims 2-3, 6-16 and 18 are rejected under 35 U.S.C 103(a) as being un-patentable over Davis-Esponda in view of Epps et al. (U.S. 6,813,243)

Regarding to claim 2:

Davis-Esponda discloses the invention substantially as disclosed in claim 1, but does not explicitly teach transferring data from an input buffer to a packet task manager; dispatching the data from the packet task manager to an analysis machine; classifying the data in the analysis machine; and modifying and forwarding the data in a packet manipulator

However, Epps teaches: transferring data from an input buffer (Fig 2, item 215) to a packet task manager (Fig 2, item 130, Col. 5, lines 50-55); dispatching the data from the packet task manager to an analysis machine (Fig 2, data travel from item 215 to 220; Col. 6, lines 33-37); classifying the data in the analysis machine (Col. 6, lines 33-37); and modifying and forwarding the data in a packet manipulator (Fig 4, item 450 and 460; Col. 6, lines); a packet manipulator (Epps, Fig 4, item 450, 460) operationally connected to said analysis machine (Epps, Fig 4, data travel from 220 to item 450 and 460).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's ideas of incorporating processes of transferring data to a packet task manager; dispatching the data from the packet task manager to an analysis machine; classifying the data in the analysis machine; modifying and forwarding the data in a packet

manipulator with Davis-Esponda's system in order to improve the communication rates, see (Epps, Col. 3, lines 39-45)

Regarding to claim 3:

Davis-Esponda discloses the invention substantially as disclosed in claim 1, but does not explicitly teach forwarding data to output after modifying

However, Epps teaches forwarding data to output after modifying (Epps, Fig. 2, item 1430; Col. 42, lines 10-21)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's ideas of modifying and forwarding the data in a packet manipulator with Davis-Esponda's system in order to improve the communication rates, see (Epps, Col. 3, lines 39-45)

Regarding to claim 6:

Davis-Esponda discloses the invention substantially as disclosed in claim 5, but does not explicitly teach an analysis machine having multiple pipelines (Epps, Fig 4, items 410-460), wherein one pipeline is dedicated to directly manipulating individual data bits of a bit field (Epps, Col. 6, lines 50-67; Col. 14, lines 1-3); a packet task manager (Epps, Fig 2, item 130, Col. 5, lines 50-55) operationally connected to said analysis machine (Epps, Fig 2, data travel from item 215 to 220; Col. 6, lines 33-37); a packet manipulator (Epps, Fig 4, item 450, 460) operationally connected to said analysis machine (Epps, Fig 4, data travel from 220 to item 450 and 460).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's ideas of co-operating processes of packet task manager;

dispatching the data from the packet task manager to an analysis machine; classifying the data in the analysis machine; modifying and forwarding the data in a packet manipulator with Davis-Esponda's system in order to improve the communication rates, see (Epps, Col. 3, lines 39-45)

Regarding to claim 7:

In addition to rejection in claim 6, Davis-Esponda- Epps further discloses multi-threaded analysis machine, see (Epps, Col. 11, lines 55-65, wherein different instructions are equivalent of multi-threaded)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's ideas of using multi-threaded analysis machine with Davis-Esponda's system in order to improve the communication rates, see (Epps, Col. 3, lines 39-45)

Regarding to claim 8:

In addition to rejection in claim 6, Davis-Esponda- Epps further discloses that analysis machine has 32 threads, although Davis-Esponda- Epps does not specifically disclose analysis machine has 32 threads, such limitations are merely a matter of design choice and would have been obvious in system of Davis-Esponda- Epps

Regarding to claim 9:

In addition to rejection in claim 6, Davis-Esponda- Epps further discloses a packet task manager (Epps, Fig 2, item 130, Col. 5, lines 50-55) operationally connected to said analysis machine (Epps, Fig 2, data travel from item 215 to 220; Col. 6, lines 33-37); a packet manipulator (Epps, Fig 4, item 450, 460) operationally connected to said analysis machine (Epps, Fig 4, data travel from 220 to item 450 and 460); a global access bus including a master

request bus (Epps, Fig 4, item 496) and a slave request bus (Epps, Fig 4, item 497) separated from each other and pipelined (Epps, Fig 4, items 410-460)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's ideas of using a global access bus including a master request bus and a slave request bus with Davis-Esponda's system in order to improve the communication rates, see (Epps, Col. 3, lines 39-45)

Regarding to claim 10:

In addition to rejection in claim 6, Davis-Esponda- Epps further discloses an external memory engine (Fig 4, item 215, external FIFO externally connected to analysis machine) operationally connected to said analysis machine (Epps, Fig 4, item 420, Col. 6, lines 30-35, wherein the analysis machine classifies packet data); a hash engine (Epps, Fig. 4, item 430; Col. 24, lines 24-28) operationally connected to said analysis machine (Epps, Col. 24, lines 24-28)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's ideas of using an external memory engine operates with analysis machine and a hash engine with Davis-Esponda's system in order to improve the communication rates, see (Epps, Col. 3, lines 39-45)

Regarding to claims 11-12:

In addition to rejection in claim 9, Davis-Esponda- Epps further discloses packet input global access bus program code (Epps: Col. 11, lines 55-60, wherein the instructions are the software code, Fig 6, item 610, 630) used for flow of data packet information from a flexible input data buffer (Epps, Fig 6, item 480) to an analysis machine (Epps, Fig 6, item 420; Col. 11,

lines 55-60; Col. 6, lines 23-37, the packet header information is retrieved and processed by the pre-process stage)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's ideas of using global access bus to control flow of data packet information with Davis-Esponda's system in order to improve the communication rates, see (Epps, Col. 3, lines 39-45)

Regarding to claim 13:

In addition to rejection in claim 9, Davis-Esponda- Epps further discloses statistics data global access bus software code (Epps: instructions residing in pipeline control Fig 4, item 495; Col. 11, lines 55-65, wherein instructions originated from pipeline control 495 dictates the-execution of the stages note, that the packet data is passed to the next stage upon completion of the current stage of execution, therefore, pipeline control is used for communications purposes between analysis machine and the packet manipulator) used for connection of an analysis machine (Fig 4, item 420) to a packet manipulator (Epps, Fig 4, item 460)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's ideas of using global access bus to control flow of data packet information with Davis-Esponda's system in order to improve the communication rates, see (Epps, Col. 3, lines 39-45)

Regarding to claim 14:

In addition to rejection in claim 9, Davis-Esponda- Epps further discloses private data global access bus software code (instructions residing in pipeline control Fig 4, item 495; Col. 11, lines 55-65, wherein instructions originated from pipeline control 495 dictates the execution

of the stages note, that the packet data is passed to the next stage upon completion of the current stage of execution, therefore, pipeline control is used for communications purposes between analysis machine and the internal memory engine) for connection of an analysis machine (Fig 4, item 420) to an internal memory engine sub-module (Epps, Fig 4, item 480, Col. 11, lines 55-65, wherein the instruction fetches

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's ideas of using private data global access bus software code for connection of an analysis machine to an internal memory engine sub-module with Davis-Esponda's system in order to improve the communication rates, see (Epps, Col. 3, lines 39-45)

Regarding to claim 15:

In addition to rejection in claim 9, Davis-Esponda- Epps further discloses lookup global access bus software code (Epps: instructions residing in pipeline control Fig 4, item 495; Col. 11, lines 55-65, wherein instructions originated from pipeline control 495 dictates the execution of the stages note, that the packet data is passed to the next stage upon completion of the current stage of execution, therefore, pipeline control is used for communications purposes between analysis machine and the internal memory engine) used for connection of an analysis machine (Fig 4, item 420) to an internal memory engine sub-module (Epps, Fig 4, item 480, Col. 1 1, lines 55-65, wherein the instruction fetches allows for connection between the PreP stage / analysis machine and the packet header buffer/ internal memory engine sub-module, look up is done through pipeline control Fig 4, item 495)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's teaching of using lookup global access bus software code for connection of an analysis machine to an internal memory engine submodule with Davis-Esponda's system in order to improve the communication rates, see (Epps, Col. 3, lines 39-45)

Regarding to claims 16:

In addition to rejection in claim 9, Davis-Esponda- Epps further discloses results global access bus software code (Epps, Col. 10, lines 5-10, the value of n is a programmable value, indicating amount of data to send to fetch stage, Fig 5, item 410) used for providing flexible access to an external memory (Epps, Col. 10, lines 5-10, amount of data received can be adjusted).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's ideas of using results global access bus software code for providing flexible access to an external memory with Davis-Esponda's system in order to improve the communication rates, see (Epps, Col. 3, lines 39-45)

Regarding to claims 18:

In addition to rejection in claim 9, Davis-Esponda- Epps further discloses a bi-directional access port operationally connected to said analysis machine (Epps, Col. 25, lines 1-7, wherein the input/output port are PPP/HDLC); an input buffer (Epps, Fig 2, item 215) operationally connected to said analysis machine (input buffer operationally connected to Prep Stage Fig 4, item 420 / analysis machine through the pipeline); and an output buffer (Epps, Fig 2, item 1430) operationally connected to said analysis machine (transmit FIFO operationally connected to Prep Stage Fig. 4, item 420 through the switch fabric).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's ideas of incorporating analysis machine, input buffer, output buffer with Davis-Esponda's system in order to improve the communication rates, see (Epps, Col. 3, lines 39-45)

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusions

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan-Dai Thi Truong whose telephone number is 571-272-7959. The examiner can normally be reached on Monday- Friday from 8:30am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob A. Jaroenchonwanit can be reached on 571-272-3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ldt
05/25/2006

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